REMARKS

By this amendment, the specification has been editorially amended, claims 16-30 have been cancelled, claims 1, 3-4, 7, 12-13, 31, 36 and 41 have been amended and new claims 43-45 have been added in the application. Currently, claims 1-15 and 31-45 are pending in the application.

The Examiner stated that claims 1-15 were objected to because it is unclear what "the platinum group" means. By this amendment, the term "the platinum group" in claims 1, 12, 31, 36 and 41 was amended to recite "an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os". The term "an elemental metal of the platinum group" in claims 3-4 was also amended to recite "the elemental metal of Pt, Pd, Rh, Ir, Ru, and Os". It is respectfully submitted that by these changes this objection has been overcome and should be withdrawn.

Claims 1-42 were rejected under 35 USC 103(a) as being obvious over Uemura (U.S. Patent No. 6,649,941) in view of Nakamura et al. (U.S. Patent No. 6,610,995).

This rejection is respectfully traversed in view of the amendments to the claims and the remarks below.

The present invention relates to semiconductor devices having micro-area (width) electrodes on nitride semiconductor layers, and particularly to high-current-driven electronic devices, such as laser diodes, high-power LEDs, FETs, and high-frequency devices. Such semiconductor devices comprise, for example, group III-V nitride semiconductors, such as GaN, AlN, and InN, including their mixed crystals AlGaN, InGaN, and AlInGa.

Specifically, a nitride semiconductor device of the present invention includes a first electrode for establishing an ohmic contact provided on a semiconductor layer and a second electrode used mainly as an extraction electrode in contact with the first electrode. The interface between the first electrode and the second electrode has a specific structure to achieve superior adhesion, low interface resistance, and stable operating characteristics.

Figs. 7A to 7C are each a schematic sectional view of a joint region between a first electrode and a second electrode of a nitride semiconductor device of the present invention. Fig. 7A shows a structure including a semiconductor layer 703 having a ridge stripe, an insulating layer 709 provided on both side surfaces and at both sides of the ridge stripe, a first electrode 705 covering the side surfaces and an upper surface of the ridge stripe, and a second electrode 706 on the first electrode 705.

Thus, the insulating layer is disposed between a) the first electrode and the second electrode and b) the semiconductor layer.

The first electrode comprises an upper layer and a lower layer. The upper layer of the first electrode is a single layer containing an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os. The elemental metal of Pt, Pd, Rh, Ir, Ru, and Os or the alloy can include homologous elements. The upper surface and lower surface of the upper layer have different functions. The upper surface makes the first electrode unreactive with ambient air and enhances the adhesion with the second electrode. The lower surface forms a stable interface with the underlying alloyed layer or lower layer to stabilize the alloying reaction.

By forming the joint region, the upper layer of the first electrode and the lower layer of the second electrode contain an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os so that the first electrode and the second electrode can adhere to each other tightly. The stability of the surface configuration (i.e. smooth surface) of the first electrode can be obtained, and the stability can be maintained even during a heat treatment which is carried out after positioning the first electrode. Further, the contact resistance

at the interface between the first electrode and the second electrode can be made low and stable. This is quite different from the prior art including Nakamura et al.

In this instance, the lower layer of the first electrode and the upper layer of the second electrode may be formed of the following materials. These materials may be used for the upper layer of the first electrode and the lower layer of the second electrode when they are formed of the same element or compound.

The lower layer of the first n electrode disposed on an n-type semiconductor layer may comprise a single-layer or multilayer film exhibiting ohmic characteristics, high adhesion and a low contact resistance, containing, for example, Ni, Co, Fe, Ti, Cu, Au, Al or an alloy of these metals. An upper layer of the second n electrode on the first n electrode may comprise a single-layer or multilayer film containing, for example, Ni, Co, Fe, Ti, Au, Al or an alloy of these metals.

By this amendment, independent claim 1 has been amended to recite "the upper layer of the first electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and the lower layer of the second electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode

and at least one of materials forming the upper layer of the first electrode and at least one of materials forming the lower layer of the second electrode are the same".

Independent claim 31 has also been amended to recite "the surface of the semiconductor layer on which the first electrode is formed comprises an electrode formation region and an insulating layer formation region, and the second electrode is disposed on the electrode formation region and the insulating layer formation region, the first electrode includes an upper layer and a lower layer, and the second electrode further includes an upper layer and a lower layer, wherein the upper layer of the first electrode and the lower layer of the second electrode each consist of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode".

These features are not shown or suggested by Uemura and Nakamura et al. or the combination of these references.

Applicants respectfully submit that Uemura and Nakamura et al. do not disclose the scope of the present invention as claimed and described below.

Uemura relates to a method of manufacturing a sealed device having a Group III nitride compound semiconductor and connectable

to an external source. More particularly, the invention is directed to a method of manufacturing a sealed flip-chip-type device and a sealed wire-bonding-type device not to be required separate sealing steps and to constitute a self-contained package which is electrically connectable to an external source.

Uemura discloses that a light transparent thin film positive electrode 310 is formed on the p-type contact layer 309 by metal deposit, and a negative electrode 340 is formed on the n^+ -layer 303. The light-transparent thin film positive electrode 310 comprises a first thin film positive electrode 311, and a second thin film positive electrode 312. The first thin film positive electrode 311, made of cobalt (Co) and having a thickness of about 15 Å, contacts to the p-type contact layer 309, and the second thin film positive electrode 312, made of gold (Au) and having a thickness of about 60 Å, contacts to the Co.

Uemura also discloses that a thick film positive electrode (pad) 320, a second thick film positive electrode 322, and a third film positive electrode 323, laminated sequentially on the light transparent thin film positive electrode 310. The first, second, and third thick film positive electrodes 321, 322, and 323 are made of vanadium (V), gold (Au), aluminum (Al), respectively, and each has thickness of about 175Å, 15,000 Å, and 100 Å.

Uemura also discloses that an optional protection layer 330 made of SiO_2 is formed on the upper surface of the device 300.

Uemura does not disclose that the upper layer of the first electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and the lower layer of the second electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode and at least one of materials forming the upper layer of the first electrode and at least one of materials forming the lower layer of the second electrode are the same as claimed in claim 1.

Uemura also does not disclose that the surface of the semiconductor layer on which the first electrode is formed comprises an electrode formation region and an insulating layer formation region, and the second electrode is disposed on the electrode formation region and the insulating layer formation region, the first electrode includes an upper layer and a lower layer, and the second electrode further includes an upper layer and a lower layer, wherein the upper layer of the first electrode and the lower layer of the second electrode each consist of an elemental metal, a compound or alloy including at least one of

Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode as claimed in claim 31.

For these reasons, it is believed that Uemura does not show or suggest the present claimed features of the present invention. Applicants also submit that Nakamura et al. do not make up for the deficiencies in Uemura.

Nakamura et al. relate to a gallium nitride-based III-V Group compound semiconductor device, and a method of producing the same.

Nakamura et al. disclose that a p-type electrode 15 is formed to directly cover substantially entire surface of the p-type semiconductor layer 13. The p-electrode is a light-transmitting, ohmic electrode comprising a metallic material. The metallic material forming the p-electrode 15 may comprise one or more metals selected from gold, nickel, platinum, aluminum, tin, indium, chromium, and titanium. A metallic material achieving preferable ohmic characteristics contains at least two metals selected from chromium, nickel, gold, titanium and platinum. A particularly preferable metallic material contains gold and nickel. Gold and nickel are preferably formed such that a layer of nickel is formed in direct contact with the p-type semiconductor layer 13, and a layer of gold is formed on the nickel layer.

Nakamura et al. also disclose that the single layer p-type electrode 15 is connected to a bonding pad 17 formed on a portion of the surface of the p-type electrode 15. Applicants respectfully submit that this single layer bonding pad is not two layer structure as claimed and it is not an electrode as disclosed and claimed in the present invention.

Nakamura et al. also disclose that the single layer bonding pad 17 is formed of gold alone, or a metallic material containing at least two metals including gold, titanium, nickel, indium and/or platinum and not containing aluminum or chromium.

Applicants respectfully submit that the even though bonding pad 17 and the p-type electrode 15 of Nakamura et al. comprise platinum, Nakamura et al. do not use platinum in multilayer electrodes. Further, in Nakamura et al., the p-type electrode 15 is directly attached to a nitride semiconductor layer 13 and therefore the contact resistance between platinum in the p-type electrode 15 and the nitride semiconductor layer 13 is high. This high contact resistance is an undesirable result and does not provide any teaching of how to improve the contact resistance as accomplished by the present invention. Also, applicants' respectfully submit that one of ordinary skill in the art would not have taken a teaching of using platinum as an electrode on a semiconductor layer with high contact resistance and a teaching

of using platinum as a bonding pad and combine them in a particular layered structure to achieve the results of the present invention.

Further, Nakamura et al. do not disclose that the upper layer of the first electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and the lower layer of the second electrode consists of an elemental metal, a compound or alloy including at least one of Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode and at least one of materials forming the upper layer of the first electrode and at least one of materials forming the lower layer of the second electrode are the same as claimed in claim 1.

Nakamura et al. also do not disclose that the surface of the semiconductor layer on which the first electrode is formed comprises an electrode formation region and an insulating layer formation region, and the second electrode is disposed on the electrode formation region and the insulating layer formation region, the first electrode includes an upper layer and a lower layer, and the second electrode further includes an upper layer and a lower layer, wherein the upper layer of the first electrode and the lower layer of the second electrode each consist of an elemental metal, a compound or alloy including at least one of

Pt, Pd, Rh, Ir, Ru and Os and form a joint region joining the first electrode to the second electrode as claimed in claim 31.

It is therefore respectfully submitted that Uemura and Nakamura et al., individually or in combination, do not teach, disclose or suggest the presently claimed invention and it would not have been obvious to one of ordinary skill in the art to combine these references to render the present claims obvious.

Applicants respectfully submit that the features claimed in independent claims 1 and 31 define over the prior art of record. Allowance of these claims is respectfully requested.

Uemura and Nakamura et al. also do not disclose many features of the dependent claims.

For example, Uemura and Nakamura et al. also do not disclose that the surface of the semiconductor layer on which the first electrode is formed comprises an electrode formation region and an insulating layer formation region and the second electrode is disposed on the electrode formation region and the insulating layer formation region as claimed in claim 7.

Uemura and Nakamura et al. also do not disclose that the semiconductor layer has a ridge and the first electrode is disposed on the upper surface of the ridge so that the nitride semiconductor device functions as a laser device as claimed in claims 9, 33 and 39.

Uemura and Nakamura et al. also do not disclose that a first insulating layer extending from the side surfaces of the ridge to the upper surface of the semiconductor layer and a second insulating layer extending from the upper surface of the first insulating layer to the side surfaces of the semiconductor layer, the second insulating layer being separate from the first electrode as claimed in claims 10, 34 and 39. Allowance of these claims is also respectfully requested.

New dependent claims 43 and 44, which directly depend from independent claims 1 and 31 respectively, have been added in the application. New dependent claims 43 and 44 recite "the lower layer of the first electrode has at least one element selected from the group consisting of Ni, Co, Fe, Cu, Au, and Al and their oxides and nitrides". Applicants respectfully submit that these additional features claimed in new claims 43 and 44 also define over the prior art of record. Allowance of these claims is also respectfully requested.

New independent claim 45 has been added in the application and is similar to claim 31. New independent claim 45 additionally recites "an insulating layer on the surface of the semiconductor layer, wherein the insulating layer is disposed between a) the first electrode and the second electrode and b) the semiconductor layer". Applicants respectfully submit that

these additional features claimed in new claim 45 also define over Uemura and Nakamura et al. and the other prior art of record. Allowance of this claim is also respectfully requested.

In view of foregoing claim amendments and remarks, it is respectfully submitted that the application is now in condition for allowance and an action to this effect is respectfully requested.

If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Respectfully submitted,

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